



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
27.03.2002 Bulletin 2002/13

(51) Int Cl.7: **H01L 23/495**

(21) Application number: **01120570.5**

(22) Date of filing: **29.08.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR
 Designated Extension States:
AL LT LV MK RO SI

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(30) Priority: **31.08.2000 JP 2000264083**
22.01.2001 JP 2001013869

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(54) **Semiconductor device having lead frame and metal plate**

(57) The present invention provides a semiconductor device whose reliability is improved by improving the adhesion strength of a metal plate or connecting chip, said plurality of electrodes and a lead frame with a molding resin. Further, the semiconductor device of the present invention prevents flow out of a conductive joining material to be employed for joining a lead terminal and the metal plate other than the joining range of the metal plate and the lead terminal, and mounts the metal

plate at high precision. In a semiconductor device (a plastic package) in which a source electrode of a semiconductor chip and source terminal of a lead frame are electrically connected by a copper plate and sealed by a resin, the surface of the copper plate is roughened to improve the adhesion strength to a molding resin. Further, a stepped part is formed in the source terminal to prevent a conductive paste from flowing out. The structure is so formed as to fit claw parts in the lead frame.

FIG. 3A

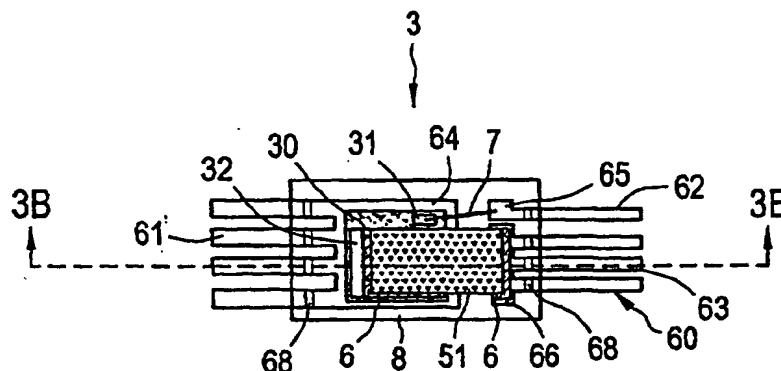
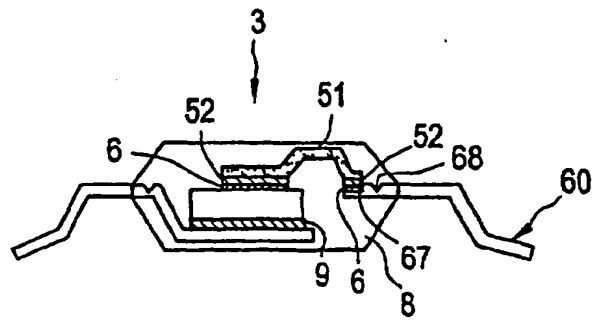


FIG. 3B



Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor device sealed with a resin, that is, a plastic package, and more particularly to a plastic package of which electrodes of a semiconductor chip and lead terminals are electrically connected to each other by a metal plate such as copper. The present application is based on Japanese Patent Application No. 264083/2000 and Japanese Patent Application No. 013869/2001, the disclosures of which are incorporated herein by reference.

2. Description of the Related Art

[0002] A semiconductor device sealed with a resin, that is, a plastic package, comprises a semiconductor chip (also called a pellet or a die), wiring materials forming outer terminals such as a lead frame, and a molding resin for sealing the semiconductor chip bonded to the wiring materials and inner leads.

[0003] Examples of the wiring materials are a tape carrier (a film carrier), a printed circuit plate, and the like other than a lead frame. As the molding resin, an epoxy resin is mainly used.

[0004] A wire bonding method has conventionally been employed in many cases as a method for electrically connecting electrodes of a semiconductor chip and lead terminals of wiring materials. FIGS. 1A and 1B are illustrations showing one example of a conventional semiconductor device 1 employing the wire bonding method. FIG. 1A is a plane view and FIG. 1B is a cross-section cut along the line I-I' of FIG. 1A.

[0005] As shown in FIGS. 1A and 1B, the semiconductor device 1 is an 8-pin SOP (Small Outline Package) produced by mounting and bonding a semiconductor chip 10 comprising a MOSFET on and with a lead frame 20, forming an electrical connection by a bonding wire 7, and sealing with a molding resin 8. The semiconductor chip 10 comprises a gate electrode 11 and three source electrodes 12 on the upper face and a drain electrode (not shown in the illustrations) on the bottom face. The lead frame 20 is provided with leads projected from opposite sides in the package; four drain leads 21 on the left side of FIG. 1A and one gate lead 22 and three source leads 23 on the right side of FIG. 1A. The drain leads 21 are integrally formed in the inside of the package and due to that, an island part 24 is formed. The gate lead 22 has an inner lead terminal part 25 (hereinafter referred to as a gate terminal) in the inside of the package. Each of three source leads 23 has an inner lead terminal part 26 (hereinafter referred to as a source terminal) in the inside of the package. The semiconductor chip 10 is bonded to the island part 24 through a die bond material 9 and the drain electrode (not shown in

the illustrations) is electrically connected with the island part 24. The gate electrode 11 on the upper face of the semiconductor chip 10 and the gate terminal 25 of the lead frame 20 are connected with each other by the bonding wire 7. Also, the source electrodes 12 and the source terminals 26 of the lead frame 20 are connected with each other by the bonding wire 7. The semiconductor chip 10, inner leads (including the island part 24, the gate terminal 25, and the source terminals 26), and the bonding wire 7 are sealed with a molding resin 8 to form a package.

[0006] The above described semiconductor device 1 is an example of a power transistor for high electric current use and in order to lower the resistance, source electrodes 12 and the gate terminal 25 are connected with the bonding wire 7 of a gold wire or the like as much as possible.

[0007] However, by the wire bonding method using a costly thin metal wire such as a gold wire or the like, problems are caused. Not only is the fabrication cost considerably increased but also disconnection takes place in the thin metal wire to make the package unsuitable for high electric current use. Recently, a method for forming an electrical connection using a metal plate such as copper has been proposed (Japanese Laid-Open Patent Application Heisei 8-148623) in a power transistor for high electric current use. As compared with a metal wire, the metal plate has advantages such as decrease of the resistance and improvement of heat radiation since the cross-sectional surface area can be widened.

[0008] However, in a plastic package in which electrodes of a semiconductor chip and the lead terminals of wiring materials are electrically connected by a metal plate, there exist the following problems.

[0009] At first, description will be given regarding an application example of a plastic package in which electrodes of a semiconductor chip and lead terminals of wiring materials are electrically connected with a metal plate. FIGS. 2A and 2B are illustrations of a semiconductor device 2 using a metal plate for connection. FIG. 2A is a plane view and FIG. 2B is a cross-section cut along the line II-II' in FIG. 2A.

[0010] As shown in FIGS. 2A and 2B, the semiconductor device 2 is an 8-pin SOP produced by mounting and bonding a semiconductor chip 30 comprising a MOSFET on and with a lead frame 40, forming an electrical connection by a bonding wire 7 and a metal plate 50 of such as a copper plate, and sealing by a molding resin 8. The semiconductor chip 30 comprises a gate electrode 31 and a single source electrode 32 with a large surface area on the upper face and a drain electrode (not shown in the illustrations) on the bottom face. The lead frame 40 is provided with leads projected from opposite sides of the package; four drain leads 41 on the left side of FIG. 2A and one gate lead 42 and three source leads 43 on the right side of FIG. 2A. The drain leads 41 are integrally formed in the inside of the pack-

age and due to that, an island part 44 is formed. The gate lead 42 has an inner lead terminal part 45 in the inside of the package. The three source leads 43 are integrally formed in the inside of the package and have a single wide width source terminal 46. The semiconductor chip 30 is bonded to the island part 44 through a die bond material 9 and the drain electrode (not shown in the illustrations) is electrically connected with the island part 44. The gate electrode 31 on the upper face of the semiconductor chip 30 and the gate terminal 45 of the lead frame 40 are connected with each other by the bonding wire 7. Also, the source electrode 32 and the source terminal 46 of the lead frame 40 are connected with each other by the metal plate 50 of copper. The metal plate 50 is bonded to the source electrode 32 in one end and to the source terminal 46 in the other end by a conductive paste 6 to electrically connect the source electrode 32 and the source terminal 46. The semiconductor chip 30, inner leads (including the island part 44, the gate terminal 45, and the source terminal 46), the bonding wire 7, and the metal plate 50 are sealed with a molding resin 8 to form a package.

[0011] As shown in FIG. 2A, the metal plate 50 is formed to have about a half width of the external size of the package and the cross-section surface area is extremely widened as compared with that of a gold wire. Consequently, the resistance of the package is lowered.

[0012] A semiconductor device is to be exposed to severe environments in which the temperature, the humidity, and the pressure are fluctuated at the time of being mounted and used after the packaging. Because the semiconductor device is repeatedly subjected to temperature alteration, the bonding of the metal plate and the molding resin occasionally becomes broken, causing separation of the metal plate from the resin. Then, water and a corrosive gas may penetrate the semiconductor chip through the parted interfaces to cause corrosion of the semiconductor chip. As a result, the reliability of the semiconductor device is lowered.

[0013] In the case of using a metal wiring, even if such separation from the molding resin occurs, since the cross-sectional surface area of a gold wire is small, the penetration route of the water and a gas is relatively narrow and therefore, water and the gas scarcely penetrate the semiconductor chip through the interface between the metal wire and the molding resin. This mitigates the extent that the reliability of the semiconductor device is deteriorated.

[0014] However, since the cross-sectional surface area of the metal plate is large as compared with that of the metal wire and further the cross-sectional surface area is intentionally widened based on the requirement of decrease of the resistance and improvement of heat radiation, the contact surface area with the molding resin is naturally widened and the penetration route of water and the gas becomes wide. This adversely affects the reliability of the semiconductor device, as it is deteriorated by the water and gas penetration.

[0015] Further, although in some cases, a solder paste and a resin type conductive paste are used for bonding the lead terminals and the metal plate, the solder paste and the conductive paste sometimes flow out of the bonding range of the metal plate and the lead terminals. In the case where the solder paste and the conductive paste flow from the lead terminals in the extended direction of the leads and are spread from the lead terminals to the package outer circumference position and to the peripheral part of the package outer circumference, the conductive paste and the like decrease the adhesion strength of the molding resin and cause the separation of the molding resin. As a result, water and the gas may easily penetrate the semiconductor chip from the outside and cause corrosion of the semiconductor chip, resulting in reduced reliability of the semiconductor device.

[0016] On the other hand, it is desired to mount a metal plate on electrodes and lead terminals of the semiconductor chip at a high precision.

[0017] The present invention has been developed while taking the above described conventional techniques into consideration. Regarding a semiconductor device (a plastic package) in which electrodes of a semiconductor chip and lead terminals are electrically connected with a metal plate, such as copper, and which is sealed with a resin, the present invention improves the sealing property of the molding resin and improves the reliability of the semiconductor device by improving the adhesion property between the metal plate and the molding resin.

[0018] Further, the present invention improves the adhesion property between the leads and the sealing resin and sealing property of the molding resin and improves the reliability of the semiconductor device by preventing a conductive bonding material employed for bonding the lead terminals and the metal plate from being spread to the outside of the bonding range between the metal plate and the lead terminals, particularly to the outside of the package on the leads.

[0019] Furthermore, the present invention provides a semiconductor device in which a metal plate is easily and highly precisely mounted on electrodes of a semiconductor chip and the lead terminals of a lead frame.

SUMMARY OF THE INVENTION

[0020] A first embodiment of the present invention to achieve the foregoing objects is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the surface of the metal plate is roughened and joined to the molding resin.

[0021] By composing such a constitution, since the surface of the metal plate is roughened, the adhesion

strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0022] Another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the surface of the metal plate is dimpled and joined to the molding resin.

[0023] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0024] Further, an additional feature of an embodiment of the present invention is the semiconductor device characterized in that the metal plate is bonded to the electrodes and the lead terminals through partial plating formed on the metal plate and the molding resin is bonded to the material of the metal plate.

[0025] By composing such a constitution, conductive bonding material to be employed for bonding the lead terminals and the metal plate is prevented from flowing out of the package on the leads and the adhesion strength between the leads and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0026] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; a lead frame having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the lead terminals have a stepped part as to form a concave shape toward the metal plate side and the lead terminals and the metal plate are joined through a conductive bonding material applied to the stepped part.

[0027] By composing such a constitution, the conductive bonding material is prevented from flowing out of the package on the leads and being spread and the adhesion strength between the leads and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0028] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; a lead frame having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that claw parts formed in the metal plate are fitted in the lead frame.

[0029] By composing such a constitution, since the surface of the metal plate has claw parts, it is possible to position the metal plate having the claw parts relative to the lead frame. Therefore, the semiconductor device can be easily manufactured with high precision.

[0030] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the roughened surface of the metal plate is joined to the molding resin: the metal plate has at least one bent part between the electrodes and the lead terminals: the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating formed on the metal plate: and that the partial plating is carried out only in the bonding parts of the metal plate to the electrodes and the lead terminals.

[0031] By composing such a constitution, since the surface of the metal plate is roughened, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0032] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the dimpled surface of the metal plate is joined to the molding resin, the metal plate has at least one bent part between the electrodes and the lead terminals, the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating formed on the metal plate, and the partial plating is carried out only in the bonding parts of the metal plate to the electrodes and the lead terminals.

[0033] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0034] Further, another embodiment of the present in-

vention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the roughened surface of the metal plate is joined to the molding resin, the metal plate has at least one bent part between the electrodes and the lead terminals, the metal plate is bonded to the electrodes and the lead terminals through the partial plating formed on the metal plate, and no plating is carried out on the parts of the metal plate to which the electrodes and the lead terminals are not bonded.

[0035] By composing such a constitution, since the surface of the metal plate is roughened, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0036] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the dimpled surface of the metal plate is joined to the molding resin, the metal plate has at least one bent part between the electrodes and the lead terminals, the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating formed on the metal plate, and no plating is carried out on the parts of the metal plate to which the electrodes and the lead terminals are not bonded.

[0037] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0038] Further, another feature of a preferred embodiment of the present invention is the semiconductor device characterized in that the lead terminals have a stepped part as to form a concave shape toward the metal plate side and the lead terminals and the metal plate are joined through a conductive bonding material applied to the stepped part.

[0039] By composing such a constitution, the conductive bonding material is prevented from flowing out on the leads and being spread and the adhesion strength between the leads and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0040] Further, another feature of a preferred embodiment of the present invention is the semiconductor device characterized in that the claw parts formed in the metal plate are fitted in the lead frame.

[0041] By composing such a constitution, since the surface of the metal plate has claw parts, it is possible to position the metal plate having the claw parts relative to the lead frame. Therefore, the semiconductor device can be easily manufactured with high precision.

[0042] Further, another feature of a preferred embodiment of the present invention is the semiconductor device characterized in that the groove parts are formed in the bent part of the metal plate in the direction crossing the extended direction of the lead terminals.

[0043] By composing such a constitution, the metal plate is made easy to be bent at the time of semiconductor device fabrication and as a result, it makes semiconductor device fabrication easy. Additionally, even if the conductive bonding material flows on the leads, the flow of the material is stopped by the groove parts. As a result, the adhesion strength between the metal plate and the molding resin is further improved and the closed property (sealed property) provided by the molding resin is further improved.

[0044] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that the groove parts are formed in the concave face side of the bent part of the metal plate.

[0045] By composing such a constitution, the metal plate is made easy to be bent at the time of semiconductor device fabrication and the closed property (sealed property) provided by the molding resin is further improved.

[0046] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that parts of the lead terminals bonded to the metal plate are partially plated.

[0047] By composing such a constitution, the oxidation preventive effect of the metal plate is further improved.

[0048] Further, another embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the surface of the metal plate is roughened and joined to the molding resin and that groove parts are formed in the lead terminals in the direction crossing the extended direction of the lead terminals themselves.

[0049] By composing such a constitution, since the surface of the metal plate is roughened, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since groove parts are formed, even if the conductive bonding material flows on the leads, the flow of the material is stopped by the groove parts and as a result, the adhesion strength between the molding resin and the leads is not deteriorated and the reliability of the semiconductor device is improved.

[0050] Further, another the other embodiment of the present invention is a semiconductor device including: a semiconductor chip having electrodes; wiring materials having lead terminals; a metal plate electrically connecting electrodes and lead terminals; and a molding resin for sealing the semiconductor chip, parts of the wiring materials, and the metal plate, characterized in that the surface of the metal plate is dimpled and joined to the molding resin and that groove parts are formed in the lead terminals in the direction crossing the extended direction of the lead terminals themselves.

[0051] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since groove parts are formed, even if the conductive bonding material flows on the leads, the flow of the material is stopped by the groove parts and as a result, the adhesion strength between the molding resin and the leads is not deteriorated and the reliability of the semiconductor device is improved.

[0052] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that the metal plate has at least one bent part between the electrodes and the lead terminals and the metal plate is bonded to the electrodes and the lead terminals through partial plating formed on the metal plate and that the partial silver plating is carried out only on the bonding parts of the metal plate to the electrodes and the lead terminals.

[0053] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0054] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that the metal plate has at least one bent

part between the electrodes and the lead terminals and the metal plate is bonded to the electrodes and the lead terminals through partial silver plating formed on the metal plate and that no plating is carried on the parts of the metal plate to which the electrodes and the lead terminals are not bonded.

[0055] By composing such a constitution, since the surface of the metal plate is dimpled, the adhesion strength between the metal plate and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved. Also, since the metal plate is bonded to the electrodes and the lead terminals through the partial silver plating, the metal plate is prevented from oxidation and the contact resistance between the electrodes and the lead terminals can be lowered.

[0056] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that the lead terminals have a stepped part as to be concave toward the metal plate and the lead terminals and the metal plate are bonded through a conductive bonding material applied to the stepped part.

[0057] By composing such a constitution, the conductive bonding material is prevented from flowing out on the leads and being spread and the adhesion strength between the leads and the molding resin is improved and the closed property (sealed property) provided by the molding resin is improved and the reliability of the semiconductor device is improved.

[0058] Further, another feature of an embodiment of the present invention is the semiconductor device characterized in that claw parts formed in the metal plate are fitted in the lead frame.

[0059] By composing such a constitution, high precision manufacturing of the semiconductor device is possible.

[0060] Further, another feature of embodiment of the present invention is the semiconductor device characterized in the groove parts are formed in the bottom face side of the bent part of the metal plate in the direction vertical to the extended direction of the lead terminals.

[0061] By composing such a constitution, even if the conductive bonding material flows out on the leads, the flow of the material is stopped by the groove parts and as a result, the adhesion strength between the molding resin and the leads is not deteriorated and the reliability of the semiconductor device is improved.

[0062] Further, another feature of embodiment of the present invention is the semiconductor device characterized in that lead terminals are partially plated in the parts bonded to the metal plate.

[0063] By composing such a constitution, the oxidation preventive effect of the metal plate is further improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0064] The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIGS. 1A and 1B are illustrations showing one example of a conventional semiconductor device 1 employing a wire bonding method. FIG. 1A is a plane view and FIG. 1B is a cross-section cut along the line I-I' of FIG. 1A;

FIGS. 2A and 2B are illustrations showing a semiconductor device 2 employing a metal plate for connection. FIG. 2A is a plane view and FIG. 2B is a cross-section cut along the line II-II' of FIG. 2A;

FIGS. 3A and 3B are illustrations showing the semiconductor device 3 of the embodiment 1 of the present invention, FIG. 3A is a plane view and FIG. 3B is a cross-section cut along the line III-III' of FIG. 3A;

FIGS. 4A to 4C are illustrations showing the copper plate 51 (example 1) to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG. 4A is a plane view, FIG. 4B is a cross-section cut along the line IV-IV' of FIG. 4A, and FIG. 4C is a bottom face of FIG. 4B;

FIGS. 5A to 5C are illustrations showing the copper plate 51 (example 2) to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG. 5A is a plane view, FIG. 5B is a cross-section cut along the line V-V' of FIG. 5A, and FIG. 5C is a bottom face of FIG. 5B;

FIGS. 6A to 6C are illustrations showing the copper plate 51 (example 3) to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG. 6A is a plane view, FIG. 6B is a cross-section cut along the line VI-VI' of FIG. 6A, and FIG. 6C is a bottom face of FIG. 6B;

FIGS. 7A to 7C are illustrations showing the copper plate 51 (example 4) to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG. 7A is a plane view, FIG. 7B is a cross-section cut along the line VII-VII' of FIG. 7A, and FIG. 7C is a bottom face FIG. 7B;

FIGS. 8A and 8B are illustrations showing the source lead 63 parts of the lead frame 60 to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG. 8A is a plane view and FIG. 8B is a side view;

FIGS. 9A and 9B are illustrations showing the semiconductor device 4 of the embodiment 2 of the present invention, FIG. 9A is a plane view and FIG. 9B is a cross-section cut along the line VIII-VIII' of FIG. 9A; and

FIGS. 10A to 10D are illustrations showing the copper plate 56 to be employed for the semiconductor device 4 of the embodiment 2 of the present inven-

tion. FIG. 10A is a plane view, FIG. 10B is a cross-section cut along the line IX-IX' of FIG. 10A, FIG. 10C is a bottom face of FIG. 10B, and FIG. 10D is a cross-section cut along the line X-X' of FIG. 10A.

BRIEF DESCRIPTION OF THE INVENTION

[0065] Preferred embodiments of a semiconductor device of the present invention will be described with reference to attached figures. Incidentally, the following descriptions are for preferred embodiments and do not restrict the present invention in any sense.

Embodiment 1

[0066] At first, a semiconductor device 3 of the embodiment 1 of the present invention will be described with reference to FIGS. 3A and 3B. FIGS. 3A and 3B are illustrations showing the semiconductor device of the embodiment 1 of the present invention. FIG. 3A is a plane view and FIG. 3B is a cross-section cut along the III-III' line in FIG. 3A.

[0067] As shown in FIGS. 3A and 3B, the semiconductor device 3 is an 8-pin SOP produced by mounting and bonding a semiconductor chip 30 composing a MOSFET on and with a lead frame 60, forming an electrical connection by a bonding wire 7, such as a gold wire, and a copper plate 51, and sealing by a molding resin 8 of such as an epoxy resin or the like. The semiconductor chip 30 comprises a gate electrode 31 and a single source electrode 32 with a large surface area on the upper face and a drain electrode (not shown in the illustrations) in the bottom face. These electrodes are aluminum or aluminum alloy electrodes, gold electrodes, or electrodes plated by gold plating, silver plating or the like. The lead frame 60 is provided with leads projected from opposite sides of the package; four drain leads 61 in the left side of FIG. 3A and one gate lead 62 and three source leads 63 in the right side of FIG. 3A. The drain leads 61 are integrally formed in the inside of the package and due to that, an island part 64 is formed. The gate lead 62 has a gate terminal 65 in the inside of the package. The three source leads 63 are integrated in the inside of the package and have an integrated single and wide source terminal 66. The semiconductor chip 30 is bonded to the island part 64 by a die bonding material 9 and a drain electrode (not shown in the illustrations) is electrically connected to the island part 64. Incidentally, the mounting region in the island part 64 of the semiconductor chip 30 may be plated with silver. The gate electrode 31 on the upper face of the semiconductor chip 30 and the gate terminal 65 of the lead frame 60 are connected by the bonding wire 7. The source electrode 32 and the source terminal 66 of the lead frame 60 are connected with the copper plate 51. The copper plate 51 is joined to the source electrode 32 in one end by a conductive paste 6 and joined to the source terminal 66 in the other end by the conductive paste 6

to electrically connect the source electrode 32 and the source terminal 66 by the copper plate 51. The semiconductor chip 30, inner leads (including the island part 64, the gate terminal 65, and the source terminal 66), the bonding wire 7, and the copper plate 51 are sealed with a molding resin 8 to form a package. The lead parts (outer leads) exposed out the molding resin 8 compose outer terminals.

[0068] The conductive paste is an adhesive containing a resin such as an epoxy resin, acrylic resin, and the like as a main agent and mixed with a curing agent and a conductive material of such as a silver powder. Although a solder paste may be used instead of a conductive paste, a conductive paste with a low elasticity is preferable to be used in order to moderate the thermal stress attributed to the difference of thermal expansion coefficients.

[0069] The copper plate 51 is made of a copper alloy. Although a metal plate of such as a Fe-Ni 42 alloy or the like may be used instead of the copper plate, a copper plate of a Cu alloy should be selected in the case where heat releasing property is required.

[0070] The copper plate 51 is a band-like thin plate having a width about a half of the outer size of the package as shown in FIG. 3A and the copper plate is so formed as to be flat in the joining face to the source electrode 32 and the joining face to the source terminal 66 and as to have two bent parts between the joining face to source electrode 32 and the source terminal 66 as shown in FIG. 3B. The copper plate 51 may be formed by pressing.

[0071] The copper plate 51 is surface-roughened in the upper face (the opposed face to the face which is to be joined to the source electrode and the source terminal) and partially plated with silver plating 52 in the bottom face.

[0072] In this case, surface roughening includes both micro-roughening (forming a roughened face at a micro level) and macro-roughening (forming a roughened face at a macro level). This is because not only roughening at a micro level but also roughening at a macro level are effective to improve the adhesion strength to the molding resin.

[0073] Consequently, it may be employed that the surface of a metal plate surface-roughened by a dimpling process of forming dimples on the surface of the metal plate is joined to the foregoing molding resin.

[0074] The surface-roughening of the metal plate may be carried out by a method for removing some parts of the material of the metal plate, a method for sticking a foreign substance to the metal plate, a method for plastically deforming the metal plate, or the like. More particularly, it can be carried out by etching, chemical polishing, a method for sticking particles such as whisker-like plating to the surface of the metal plate, a sand blast method, a method for transferring the uneven surface of a die, or the like.

[0075] Further, in case of plating the copper plate 51

as the metal plate, it is effective to carry out partial plating on the joining face of the metal plate to the electrodes of the semiconductor chip and on the joining face of the metal plate to the lead terminals but not on the entire surface of the metal plate. This is because if plating is carried out on the joining face of the metal plate to the molding resin, the metal plate surface is smoothed to decrease the adhesion strength to the molding resin. That is, the foregoing metal plate is joined to the foregoing electrodes and the foregoing lead terminals through the partial plating formed on the foregoing metal plate and the foregoing molding resin is joined to the material of the foregoing metal plate.

[0076] More details on these features will be described with reference to FIGS. 4A to 4C, FIGS. 5A to 5C, FIGS. 6A to 6C, and FIGS. 7A to 7C. FIGS. 4A to 4C are illustrations of the copper plate 51 (example 1) to be employed for the embodiment 1 of the semiconductor device 3 of the present invention. FIG. 4A is the illustration of the upper face, FIG. 4B is a cross-section cut along the line IV-IV' in FIG. 4A, and FIG. 4C is the illustration of the bottom face.

[0077] As illustrated in FIGS. 4A and 4B, the copper plate 51 has dimples 53 in the upper face. The dimples 53 are those formed in the copper plate 51 and can be formed by etching and pressing. In the case of forming them by etching, they are formed by half etching, which is incompletely carried out etching. In the case where etching is completely carried out, the amount of copper removed is increased and the resistance value of the copper plate 51 is increased. In the case where the copper plate 51 has nothing to do with the resistance value, etching may completely be carried out and through holes may be formed instead of the dimples 53. That is because the adhesion strength to the molding resin 8 can be improved by through holes.

[0078] Further, the bottom face of the copper plate 51 is formed with silver plating 52. The silver plating 52 is for preventing oxidation of the copper plate 51, maintaining the conductivity, and lowering the contact resistance between the source electrode 32 and the source terminal 66. As illustrated in FIGS. 4B and 4C, the silver plating 52 is not carried out on the whole surface of the bottom of the copper plate 51 but on the joining faces to the source electrode 32 and to the source terminal 66. On the other hand, no silver plating is carried out on the upper face of the copper plate 51.

[0079] The silver plating is preferably carried out only on the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. Further, it is preferable that no silver plating is carried out on the copper plate 51 other than the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. In such a manner, the adhesion strength of the copper plate 51 and the molding resin 8 is improved and as a result, the reliability of the semiconductor device can further be improved.

[0080] Further, the silver plating may be carried out

on the joining part of the source terminal 66 to the copper plate 51. The oxidation preventive effect of the copper plate 51 can further be improved by plating the source terminal 66 with silver in such a manner.

[0081] By sealing the copper plate 51 having the above described structure with a resin in the state as shown in FIGS. 3A and 3B, some of the molding resin 8 fills the dimples 53 and is hardened, so that the adhesion strength of the copper plate 51 and the molding resin 8 is improved and the reliability of the semiconductor device 3 is improved.

[0082] The structures as illustrated in FIGS. 5A to 5C and FIGS. 6A to 6C may be employed as the structure of the surface-roughened copper plate 51. FIGS. 5A to 5C show a copper plate 51 (example 2) to be employed for the embodiment 1 of the semiconductor device 3 of the present invention. FIG. 5A is the illustration of the upper face, FIG. 5B is a cross-section cut along the line V-V' in FIG. 5A, and FIG. 5C is the illustration of the bottom face.

[0083] As illustrated in FIGS. 5A and 5B, the copper plate 51 is roughened in the upper face by a sand blast method or a chemical polishing method. That is, the copper plate 51 has a roughened face 54 in the upper face. By sealing the copper plate 51 having the above described structure with a resin in the state as shown in FIGS. 3A and 3B, the molding resin 8 is joined to the material of the copper plate 51 and some of the molding resin 8 fills the fine recessed parts of the roughened face 54 and is hardened, so that the adhesion strength of the copper plate 51 and the molding resin 8 is improved and the reliability of the semiconductor device 3 is improved.

[0084] Further, the bottom face of the copper plate 51 is plated with silver 52. The silver plating 52 is for preventing oxidation of the copper plate 51, maintaining the conductivity, and lowering the contact resistance between the source electrode 32 and the source terminal 66. As illustrated in FIGS. 5B and 5C, the silver plating 52 is not carried out on the whole surface of the bottom of the copper plate 51 but on the joining faces to the source electrode 32 and to the source terminal 66. On the other hand, no silver plating is carried out on the upper face of the copper plate 51.

[0085] The silver plating is preferably carried out only on the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. Further, it is preferable that no silver plating is carried out on the copper plate 51 other than the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. In such a manner, the adhesion strength of the copper plate 51 and the molding resin 8 is improved and as a result, the reliability of the semiconductor device can further be improved.

[0086] Further, the silver plating may be carried out on the joining part of the source terminal 66 to the copper plate 51. The oxidation preventive effect of the copper plate 51 can further be improved by plating the source terminal 66 with silver in such a manner.

[0087] FIGS. 6A to 6C illustrate a copper plate 51 (example 3) to be employed for the embodiment 1 of a semiconductor device 3 of the present invention. FIG. 6A is the illustration of the upper face, FIG. 6B is a cross-section cut along the line VI-VI' in FIG. 6A, and FIG. 6C is the illustration of the bottom face.

[0088] As illustrated in FIG. 6A and 6B, whisker plating 55 adheres to and is fixed on the upper face of the copper plate 51. By sealing the copper plate 51 having the above described structure with a resin in the state as shown in FIG. 3, the molding resin 8 is joined to the material of the copper plate 51 and fills even the fine surroundings of the whisker plating 55 and is hardened, so that the adhesion strength of the copper plate 51 and the molding resin 8 is improved and the reliability of the semiconductor device 3 is improved.

[0089] Further, the bottom face of the copper plate 51 is plated with silver 52. The silver plating 52 is for preventing oxidation of the copper plate 51, maintaining the conductivity, and lowering the contact resistance between the source electrode 32 and the source terminal 66. As illustrated in FIGS. 6B and 6C, the silver plating 52 is not carried out on the whole surface of the bottom of the copper plate 51 but on the joining faces to the source electrode 32 and to the source terminal 66. On the other hand, no silver plating is carried out on the upper face of the copper plate 51.

[0090] The silver plating 52 is preferably carried out only on the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. Further, it is preferable that no silver plating is carried out on the copper plate 51 other than the joining parts of the copper plate 51 to the source electrode 32 and the source terminal 66. In such a manner, the adhesion strength of the copper plate 51 and the molding resin 8 is improved and as a result, the reliability of the semiconductor device can further be improved.

[0091] Further, the silver plating may be carried out on the joining part of the source terminal 66 to the copper plate 51. The oxidation preventive effect of the copper plate 51 can further be improved by plating the source terminal 66 with silver in such a manner.

[0092] Further, regardless of whether the above described dimples 53, roughened surface 54, and whisker plating 55 are formed or not, the molding resin 8 is joined to the material of the copper plate 51, the oxygen group on the surface of the copper plate 51 improves the adhesion strength to the molding resin 8 and the reliability of the semiconductor device 3 can be improved.

[0093] FIGS. 7A to 7C illustrate a copper plate 51 (example 4) to be employed for the embodiment 1 of a semiconductor device 3 of the present invention. FIG. 7A is the illustration of the upper face, FIG. 7B a cross-section cut along the line VII-VII' in FIG. 7A, and FIG. 7C is the illustration of the bottom face.

[0094] As illustrated in FIGS. 7B and 7C, groove parts 70 are formed in two bent parts of the copper plate 51 in the direction crossing the extended direction of the

source terminal 66. These groove parts 70 can be formed by etching and press working. By forming such groove parts 70, the copper plate 51 is made easy to be bent at the time of fabricating the semiconductor device 3 and consequently the fabrication of the semiconductor device is made easy. Also, the adhesion strength between the copper plate 51 and the molding resin 8 is further improved, the closed property (sealed property) provided by the molding resin is further improved and the reliability of the semiconductor device 3 is further improved.

[0095] In FIGS. 7A to 7C, the groove parts 70 are formed in the recessed face side of the bent parts of the foregoing metal plate, the groove parts 70 may be formed in the side opposed to the recessed face side of the bent parts, in other words, in the projected face side.

[0096] On the other hand, as illustrated in FIGS. 3A and 3B, a stepped part 67 to form a recessed part toward the copper plate 51 side and a groove part 68 are formed in the lead frame 60. That will be described with reference to FIGS. 8A and 8B. FIGS. 8A and 8B are partial illustrations of a source lead 63 part of the lead frame 60 to be employed for the embodiment 1 of a semiconductor device 3 of the present invention. FIG. 8A is the plane view and FIG. 8B is a side view.

[0097] As illustrated in FIGS. 8A and 8B, the stepped part 67 is formed in the source terminal 66. The source terminal 66 is so formed as to be wide and integrate three source leads. That is, is formed to be long in the same direction as that of the package external shape 81. As illustrated in FIGS. 8A and 8B, the stepped part 67 is a stepped part to be recessed toward the copper plate 51 side from the lead upper end in the surrounding. In the case of the observation of the source leads along the extended direction of the lead from the source terminal 66 as the base point, a rising wall face 67a is formed. The wall face 67a is parallel to the package external shape 81 and vertical to the extended direction of the source leads 63.

[0098] Further, groove parts 68 are formed in the respective three source leads 63. As illustrated in FIGS. 8A and 8B, each groove 68 is a V-shape groove parallel to the package external shape 81 and vertical to the extended direction of the source lead 63.

[0099] Since the above described stepped part and groove parts are not formed in a conventional lead frame, during a series of processes of applying a solder paste or a conductive paste is printed on or applied to the source terminal, mounting a metal plate thereon, and reflowing or curing the paste, the solder paste or the conductive paste sometimes flows toward the outside of the package on the source lead and is spread near the package external shape 81 or to the outside of the package external shape 81. Consequently, the adhesion strength of the source leads and the molding resin is deteriorated and the reliability of the semiconductor device is decreased.

[0100] However, in the semiconductor device 3 of the

embodiment of the present invention, since the stepped part 67 and the groove parts 68 are formed in the lead frame 60, the solder paste or the conductive paste printed on or applied to the bottom face of the stepped part 67 is inhibited from flowing on the source leads and being spread by the stepped part 67 and the wall face 67a. Also, by any chance, even if the solder paste or the conductive paste flows out over the wall face 67a, the flow can be intercepted by the groove parts 68. As a result, the adhesion strength of the source leads 63 and the molding resin 8 is not deteriorated and the reliability of the semiconductor device is improved.

[0101] The stepped part 67 and groove parts 68 can be formed at the time of the pressing process of the lead frame. The stepped part 67 is a stepped part formed by crushing a part of the source terminal 66 at the time of the pressing process, however the stepped part may be formed by bending without crushing.

[0102] Further, instead of the stepped part 67, a groove with an approximately U-shape cross section may be formed in the same position of the stepped part 67. However, in the case of forming the groove, if a solder paste or a conductive paste overflows the groove part, the solder or conductive paste possibly flows toward the outside of the package on the source leads 63, so that it is advantageous to form the above described stepped part. That is because, in the case of forming a stepped part, there is no wall face to inhibit the flow of the solder paste or the conductive paste in the inner side of the package and hence the excess solder paste or the conductive paste flows to the inner side of the package.

[0103] The stepped parts are made to be lowered stepped parts relative to an adjacent segment of the plate. That is because if they are made to be elevated stepped parts, the wall faces formed are only wall faces seen descending by the observation along the extended direction of the lead from the lead terminals from the base points. Such descending wall faces cannot inhibit the flow of the conductive joining material on the lead.

[0104] Further, since some of the molding resin 8 fills the groove parts 68 and is cured in the groove parts 68, the adhesion strength of the lead frame 60 and the molding resin 8 is improved by the groove parts 68 formed in the lead frame. Therefore, as illustrated in FIGS. 3A and 3B, groove parts 68 are formed in the drain leads 61 and the gate lead 62 the inner side near the package terminal face.

Embodiment 2

[0105] Next, an embodiment 2 of a semiconductor device 4 of the present invention will be described with reference to FIGS. 9A and 9B and FIGS. 10A to 10C. FIGS. 9A and 9B are illustrations showing the semiconductor device 4 of the embodiment 2 of the present invention and FIG. 9A is a plane view and FIG. 9B is a cross-section cut along the VIII-VIII' line in FIG. 9A. FIGS. 10A to

10C are illustrations showing a copper plate 56 to be employed for the semiconductor device 4 of the embodiment 2 of the present invention. FIG. 10A is a plane view, FIG. 10B is a cross-section cut along the IX-IX' line in FIG. 10A, and FIG. 10C is the bottom FIG..

[0106] The semiconductor device 4 of the embodiment 2 has the same constitution as that of the semiconductor device 3 of the embodiment 1. However, it is different in the point that claw parts 58 are formed in the copper plate 56.

[0107] Similar to the copper plate 51 in the embodiment 1, the copper plate 56 is plated with silver plating 57a, 57b. As illustrated in FIGS. 10B and 10C, the silver plating 57a, 57b is not carried out on the entire bottom face of the copper plate 56 but the silver plating 57a is carried on the joining face to the source electrode 32 and the silver plating 57b is carried out on the joining face of the source terminal 66. On the other hand, no silver plating is carried out on the upper face of the copper plate 56.

[0108] Although the copper plate 56 has the same shape as that of the copper plate 51 of the embodiment 1, three claw parts 58 are extended in the end part of the copper plate 56 in the source lead 63 side. As illustrated in FIG. 9B, the three claw parts 58 are formed by bending the copper plate 56 toward the bottom face and protruded beyond the face plated with silver 57b. In FIGS. 9A and 9B, the second and the third claw parts 58 from the top are fitted in the intervals of the three source leads 63. In FIGS. 9A and 9B, the first claw part 58 from the top is fitted in the interval between the gate lead 62 and the source lead 63 but is not brought into contact with the gate lead 62 and isolated from the gate lead 62 and together with other claw parts 58, the first claw part 58 is fitted in the source lead 63.

[0109] These claw parts 58 can be formed at the time of pressing process of the copper plate 56.

[0110] Attributed to the formation of the above described claw parts 58, the copper plate 56 can be positioned at high precision on the source electrode 32 and the source terminal 66 of a semiconductor chip 30 by inserting the claw parts 58 among leads and fitting in the source leads 63 at the time of mounting the copper plate 56. It is preferable to form two or more claw parts. If there is only one, engagement among the leads is carried out only at one point. Consequently, rotation of the metal plate around the claw part as a supporting point may occur, resulting in a positioning difference of the metal plate.

[0111] Hereinafter, examples of copper plates with the surface average roughness Ra will be disclosed.

[0112] The surface of a copper plate without being subjected to surface-roughening had an average surface roughness of 0.1 μm Ra.

[0113] The surface of a copper plate subjected to surface-roughening by chemical polishing (chemical solution treatment) had an average surface roughness of 0.2 to 0.3 μm Ra. The surface of a copper plate subjected

to surface-roughening by a sand blast method had an average surface roughness of 0.3 to 0.4 μm Ra. The surface of a copper plate subjected to surface-roughening by whisker-like plating had an average surface roughness of 0.3 to 0.4 μm Ra.

[0114] As described above, the present invention is effective to improve the adhesion strength of a metal plate and a molding resin since the molding resin is joined to the surface of a surface roughened metal plate and also effective to prevent flow out of a conductive joining material since a stepped part to be recessed toward the metal plate side is formed in the lead terminal part to be coated with the joining material and as a result, the present invention is effective to improve the adhesion strength of the molding resin and the closed property (sealed property) provided by the molding resin, to prevent the penetration of the semiconductor chip with water, a gas, or the like and to improve the reliability of the semiconductor device.

[0115] Further, the present invention is effective to mount a metal plate on electrodes of the semiconductor chip and the lead terminals of the lead frame easily at high precision attributed to the structure in which the claw parts formed in the metal plate are fitted in the lead frame.

[0116] The present invention is not limited to the above embodiments, and it is contemplated that numerous modifications may be made without departing from the spirit and scope of the invention. The semiconductor device, as described above with reference to the FIGS., is a merely an exemplary embodiment of the invention, and the scope of the invention is not limited to these particular embodiments. Accordingly, other structural configurations may be used, without departing from the spirit and scope of the invention as defined in the following claims.

Claims

1. A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;
wiring materials having a plurality of lead terminals;
a metal plate connecting with said plurality of electrodes at a first portion of said metal plate and connecting with said plurality of lead terminals at a second portion of said metal plate; and
a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein
a surface of said metal plate is uneven and joined to said molding resin.

2. The semiconductor device as claimed in claim 1 wherein said metal plate connects with said plurality

- of electrodes and said plurality of lead terminals by a plating formed on said metal plate.
3. The semiconductor device as claimed in claim 2 wherein said metal plate has at least one bent part between said first portion and said second portion, and
wherein said plating is formed on said first portion and said second portion.
 4. The semiconductor device as claimed in claim 3 wherein said plating is formed only on said first portion and said second portion.
 5. The semiconductor device as claimed in claim 4 wherein said metal plate has a groove formed at said bent part in a direction crossing a direction of said lead terminals.
 6. The semiconductor device as claimed in claim 5 wherein said groove is formed in a recessed face side of said bent part of said metal plate.
 7. The semiconductor device as claimed in claim 3 wherein said plurality of lead terminals are plated.
 8. The semiconductor device as claimed in claim 3 wherein said plurality of lead terminals have a concave, and
wherein said metal plate are connected with said concave by a conductive bonding material.
 9. The semiconductor device as claimed in claim 8 wherein said surface of said metal plate is roughened.
 10. The semiconductor device as claimed in claim 8 wherein said surface of said metal plate is dimpled.
 11. The semiconductor device as claimed in claim 8 wherein said metal plate has at least one through hole.
 12. The semiconductor device as claimed in claim 8 wherein said surface of said metal plate has a plurality of whisker platings.
 13. The semiconductor device as claimed in claim 3 wherein said metal plate has claw parts fitted in said wiring materials.
 14. The semiconductor device as claimed in claim 13 wherein said surface of said metal plate is roughened.
 15. The semiconductor device as claimed in claim 13 wherein said surface of said metal plate is dimpled.
 16. The semiconductor device as claimed in claim 13 wherein said metal plate has at least one through hole.
 17. The semiconductor device as claimed in claim 13 wherein said surface of said metal plate has a plurality of whisker platings.
 18. A semiconductor device comprising:
a semiconductor chip having a plurality of electrodes;
wiring materials having a plurality of lead terminals;
a metal plate connecting with said plurality of electrodes at a first portion of said metal plate and connecting with said plurality of lead terminals at a second portion of said metal plate by a plating formed on said metal plate, said metal plate having at least one bent part between said first portion and said second portion and a groove formed at said bent part in a direction crossing a direction of said lead terminals; and
a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein
a surface of said metal plate is uneven and joined to said molding resin.
 19. The semiconductor device as claimed in claim 18 wherein said surface of said metal plate is roughened.
 20. The semiconductor device as claimed in claim 18 wherein said surface of said metal plate is dimpled.

FIG. 1A
RELATED ART

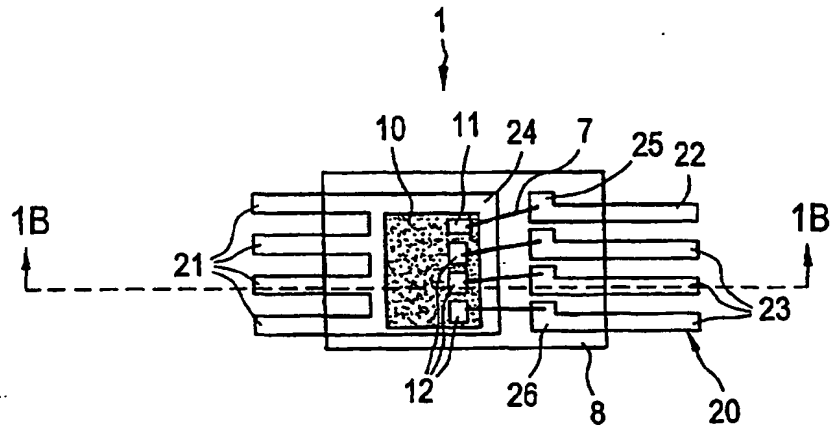


FIG. 1B
RELATED ART

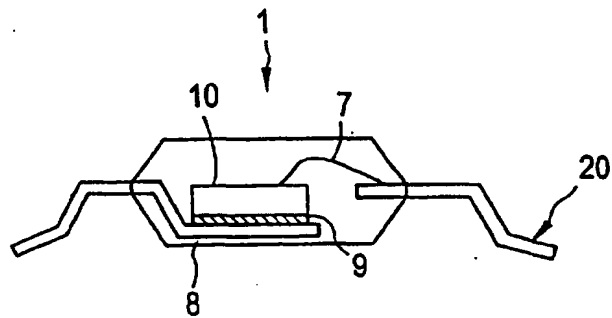


FIG. 2A
RELATED ART

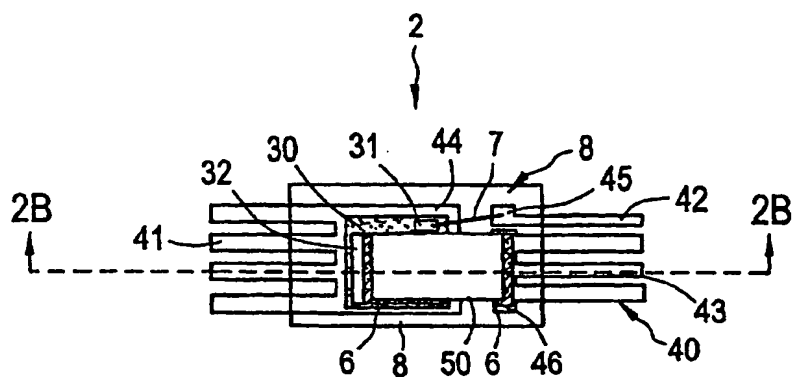


FIG. 2B
RELATED ART

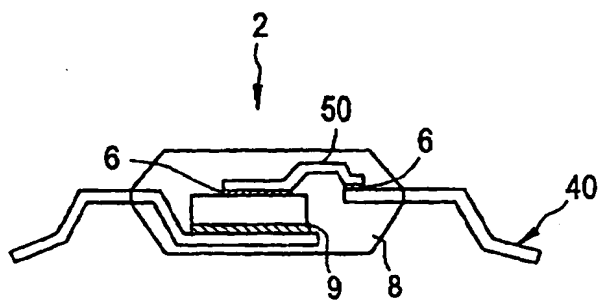


FIG. 3A

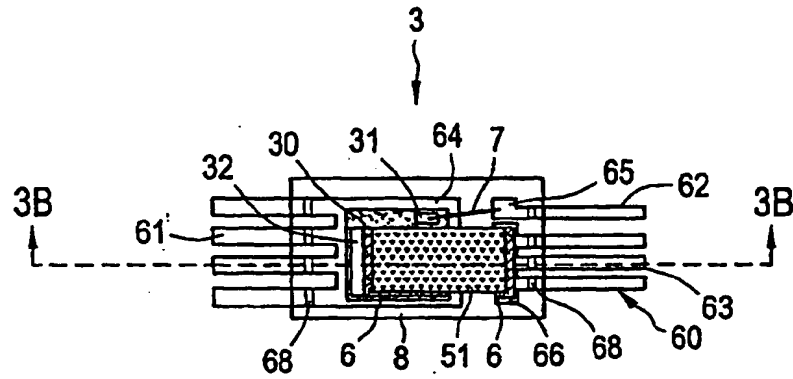
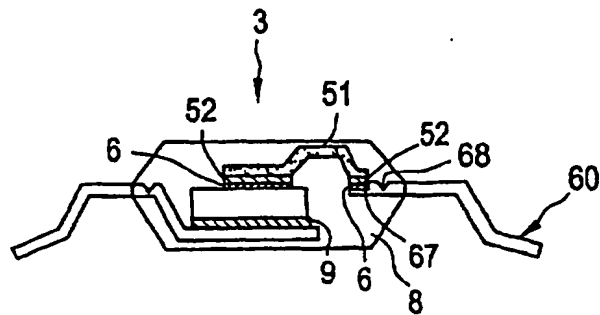
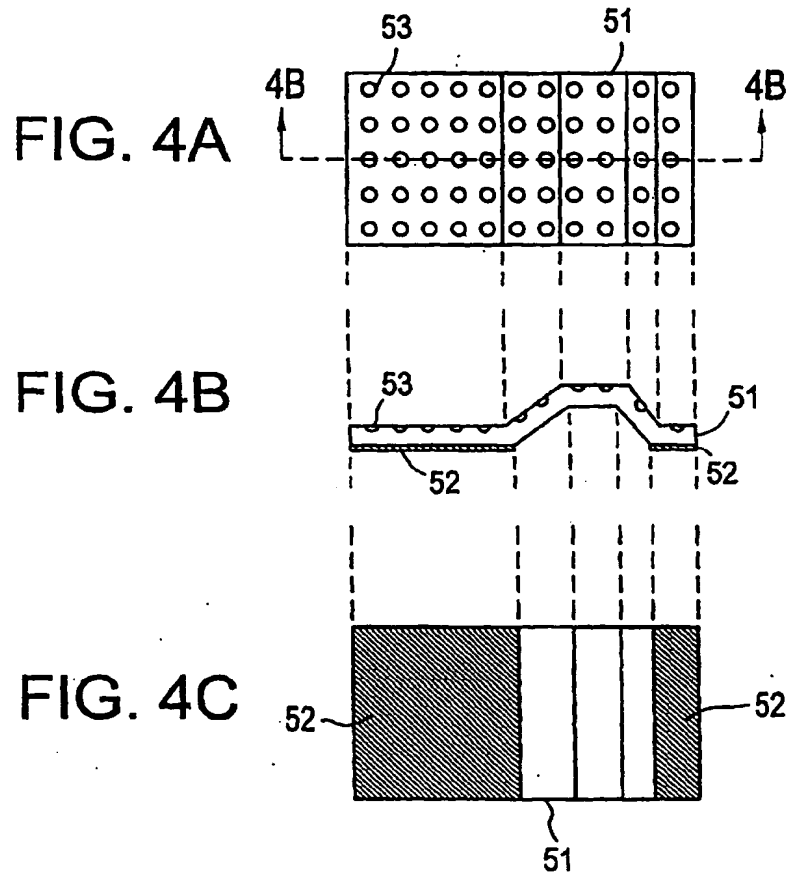
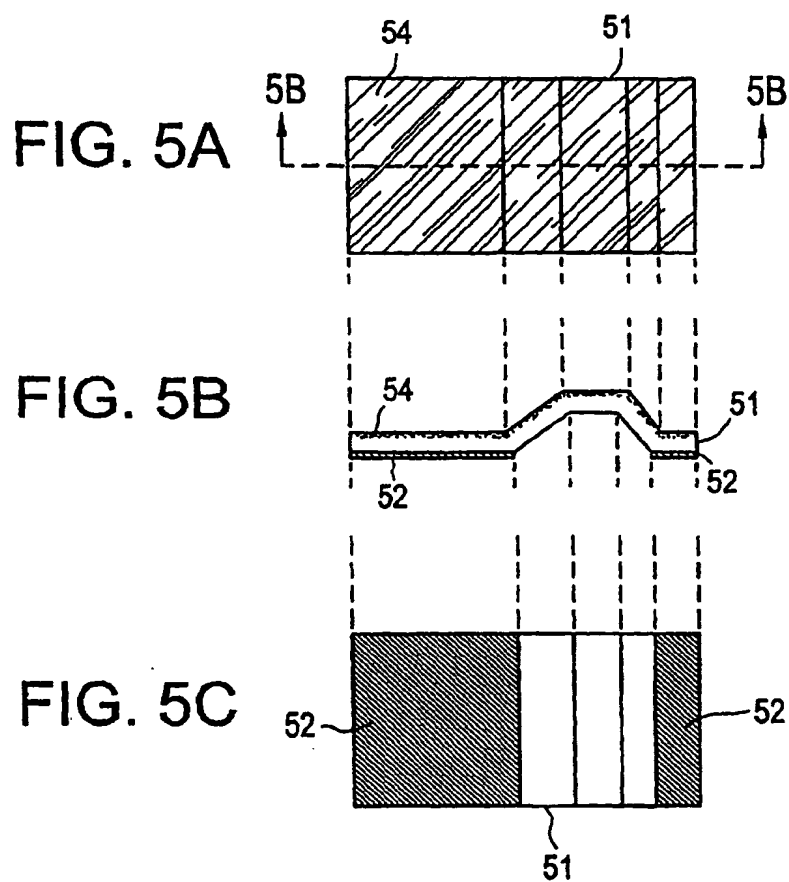
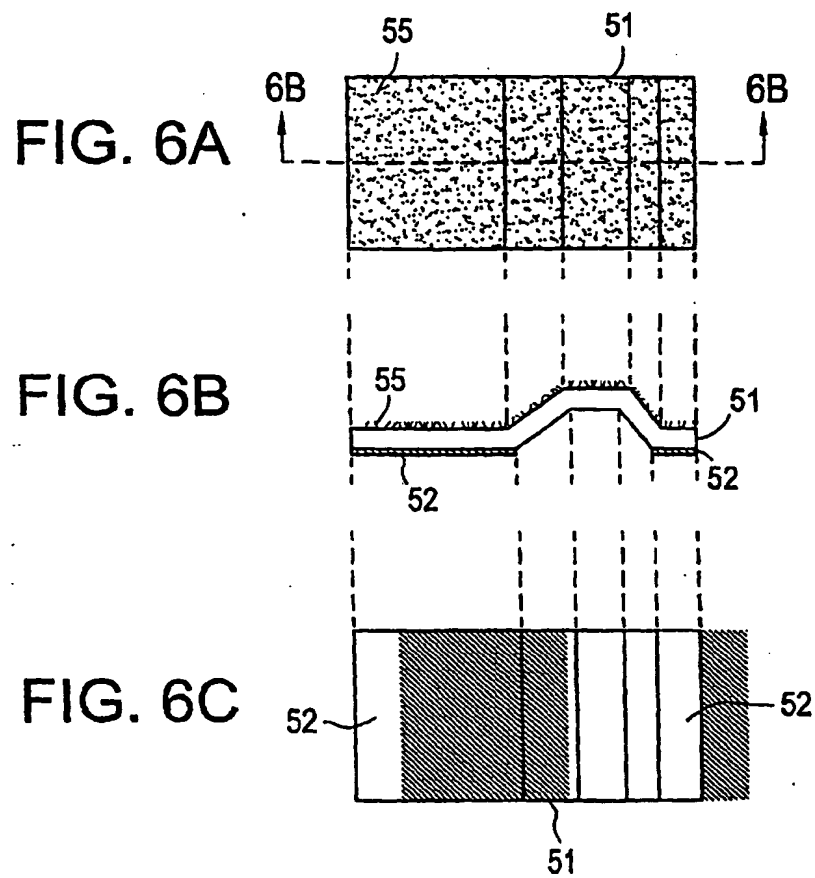


FIG. 3B









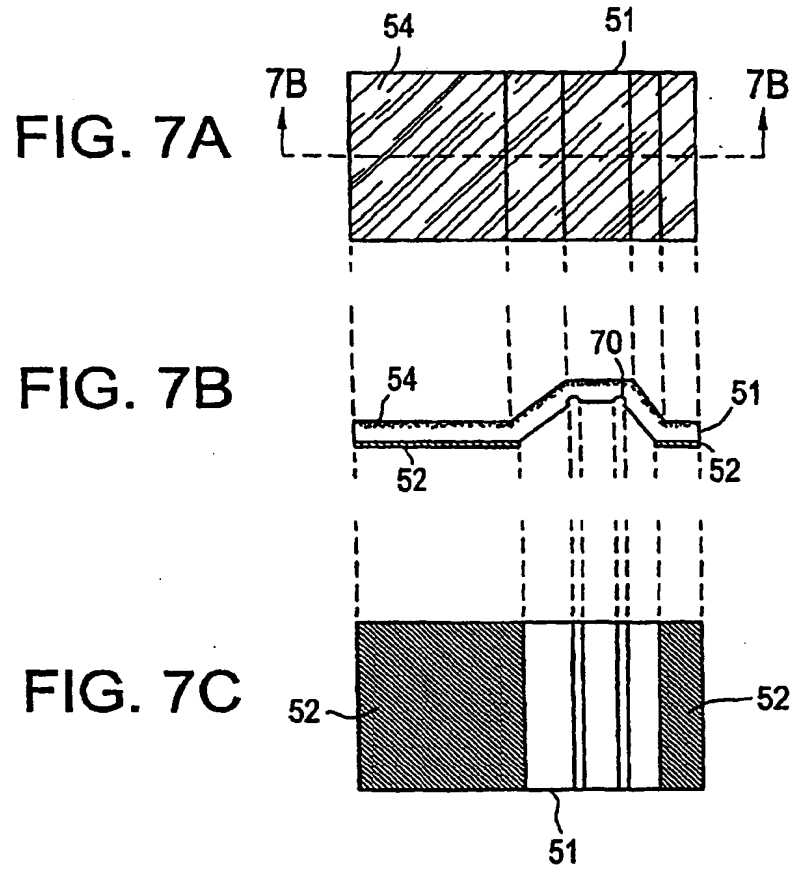


FIG. 8A

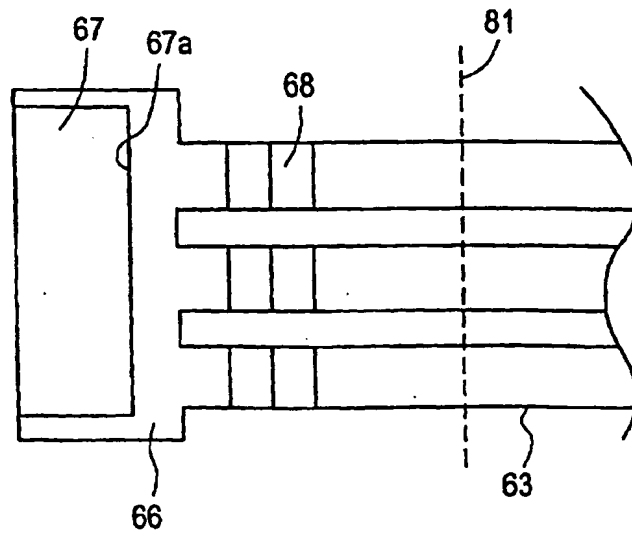


FIG. 8B

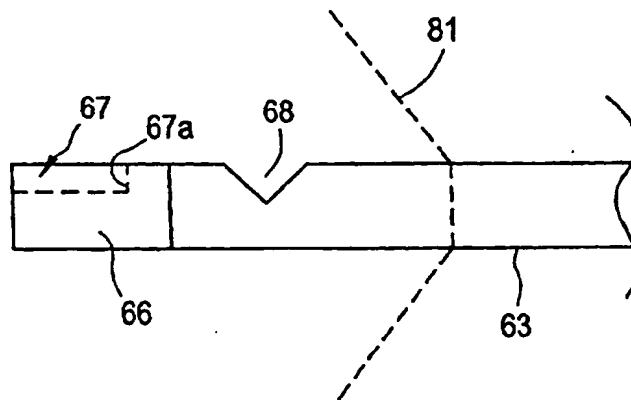


FIG. 9A

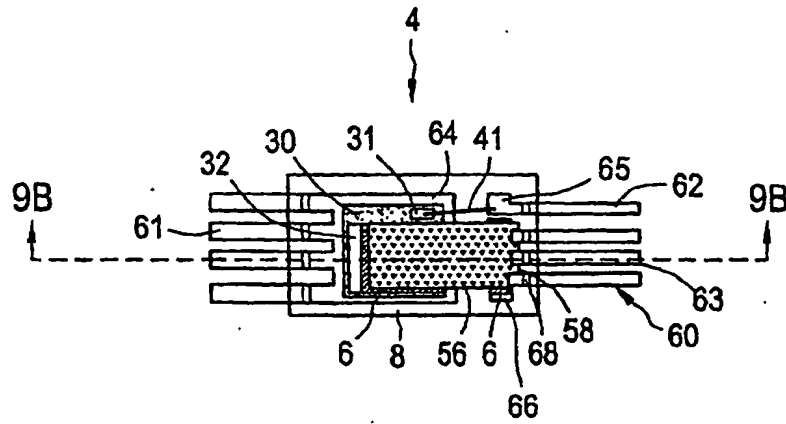


FIG. 9B

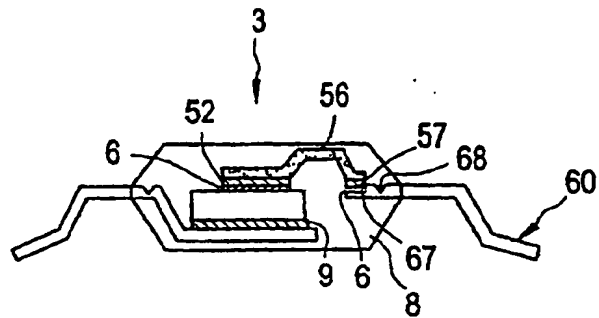


FIG. 10A

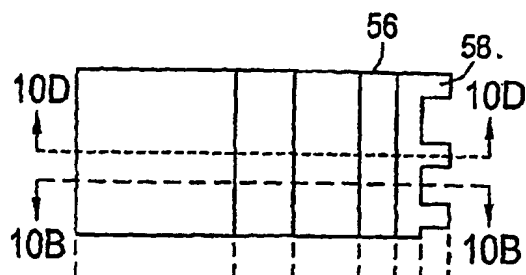


FIG. 10B

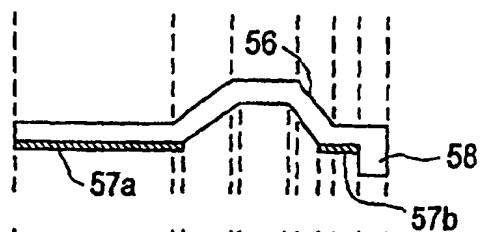


FIG. 10C

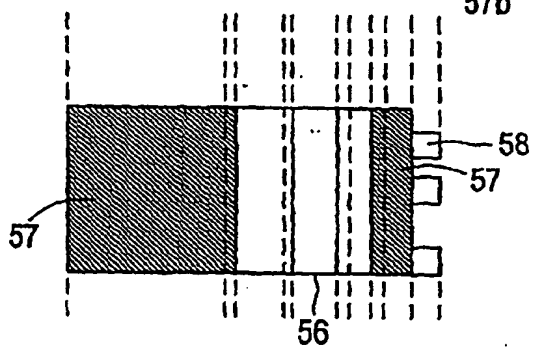


FIG. 10D

